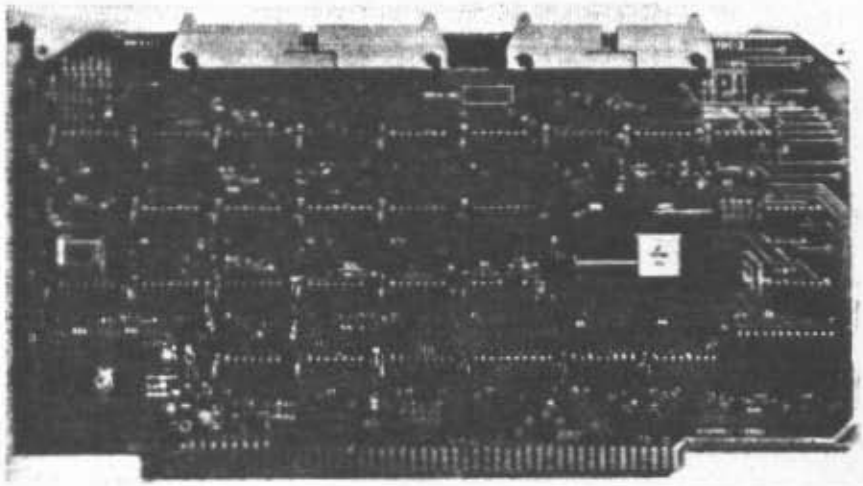
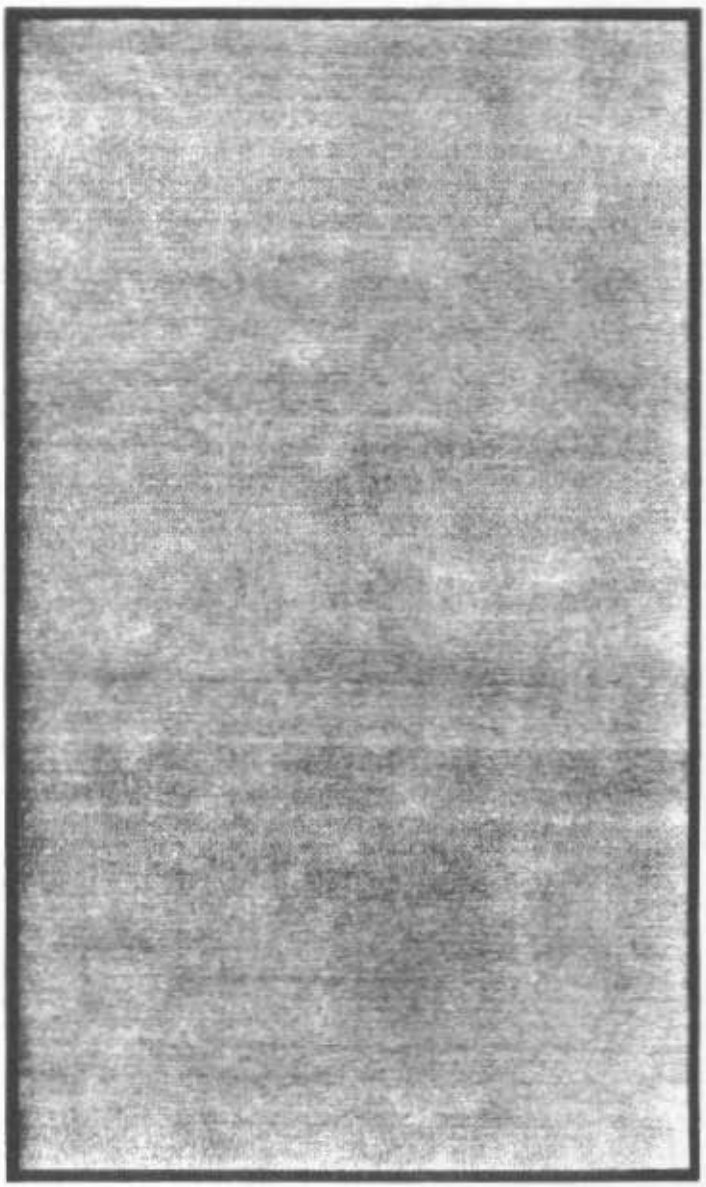
FDC·3
CARD USER'S GUIDE

TEI INC.





FDC-3

FLOPPY-DISK CONTROLLER

USER MANUAL

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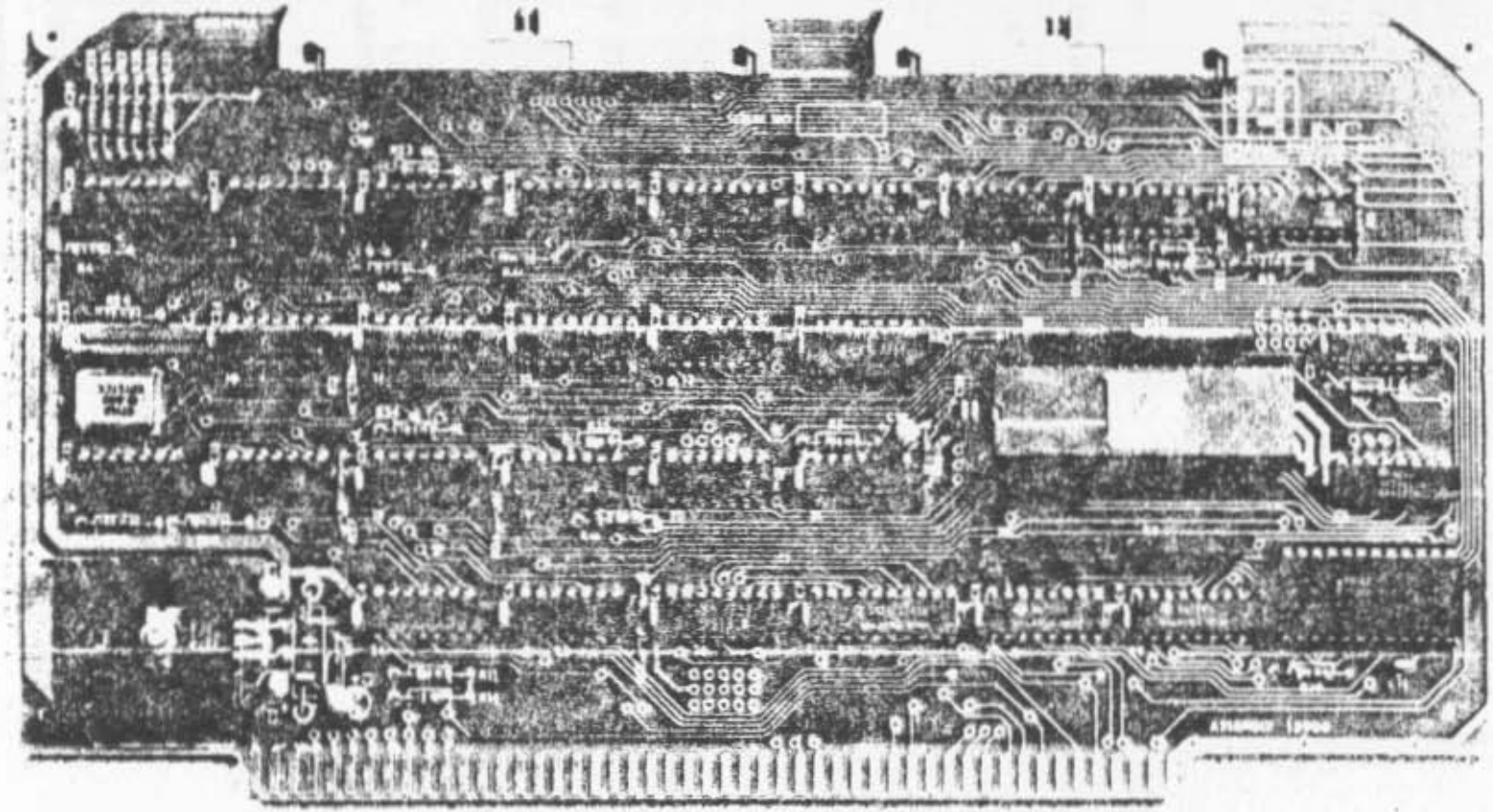


FIGURE 1-1 TEI, Inc. FDC-3 Floppy-Disk Controller

SECTION I

INTRODUCTION

1.1 GENERAL

The TEI, Inc. FDC-3 Floppy-Disk Controller combines the 1791 LSI floppy-disk controller device and supporting logic to control up to eight standard drives and up to three mini drives - single or double-sided, single or double density. The 1791 device allows software selection of both density and number of sides for ease in changing system configuration.

The FDC-3 Floppy-Disk Controller also offers such features as IBM-compatible formats; buffered control, data, and status lines; automatic track-seek with verification; and CRC generation and detection.

The TEI, Inc. FDC-3 Floppy-Disk Controller was specifically designed to operate reliably in a TEI, Inc. Computer System using TEI, Inc. system components. Although the FDC-3 Floppy-Disk Controller may work properly in another manufacturer's computer, or with another manufacturer's components, TEI, Inc. cannot guarantee that it will do so.

1.2 PHYSICAL DESCRIPTION

The FDC-3 Controller card (Figure 1-1) consists of 31 integrated circuits, plus supporting components; 50-pin socket for standard (8") diskette-drive signal cable; and a 34-pin socket for miniature (5.25") drive signal cable; all mounted on a 5" x 10" (127-mm x 254-mm) fiberglass double-sided etched-circuit board complete with a standard S-100 bus connector that has gold-plated contacts for reliability and long life.

SECTION II

INSTALLATION

1) Turn System power off.

CAUTION! NEVER INSTALL OR REMOVE A CIRCUIT CARD WITH POWER ON!

2) Install card in any card slot. If the FDC-3 card replaces an FDC-2 card, install in same slot to avoid having to move cables. Note that the edge-connector location prevents plugging the card in backwards.

3) Plug signal cable(s) into FDC-3 card. Cable from standard (8") drive(s) plugs into large connector. Cable from miniature (5.25") drive(s) plugs into small connector. Be sure connector(s) firmly seated.

4) Turn System on, with all drive doors open. If T/DOS Version 1.44 (or lower) information appears (after CRT warmup) with drive doors open, FDC-3 card will not work properly.

5) Place System diskette[1] in drive A[2], close drive door, wait for memory-size prompt, then enter size (in K) for desired program, or press RETURN to load maximum size automatically.

6) Check CRT Display. If T/DOS Version 2.0 (or higher) installed, System is ready for operation.

---

[1] Consult local documentation, Supervisor, or Dealer for correct diskette insertion method on your System. Diskette should not be Write-Protected, if recording on diskette required.

[2] TEI, Inc. Systems with eight function keys on keyboard, can load T/DOS Version 2.0 (or higher) from drives B, C, or D, if desired. Press key 8 to load from drive B, key 7 to load from drive C, keys 7 and 8 to load from drive D.

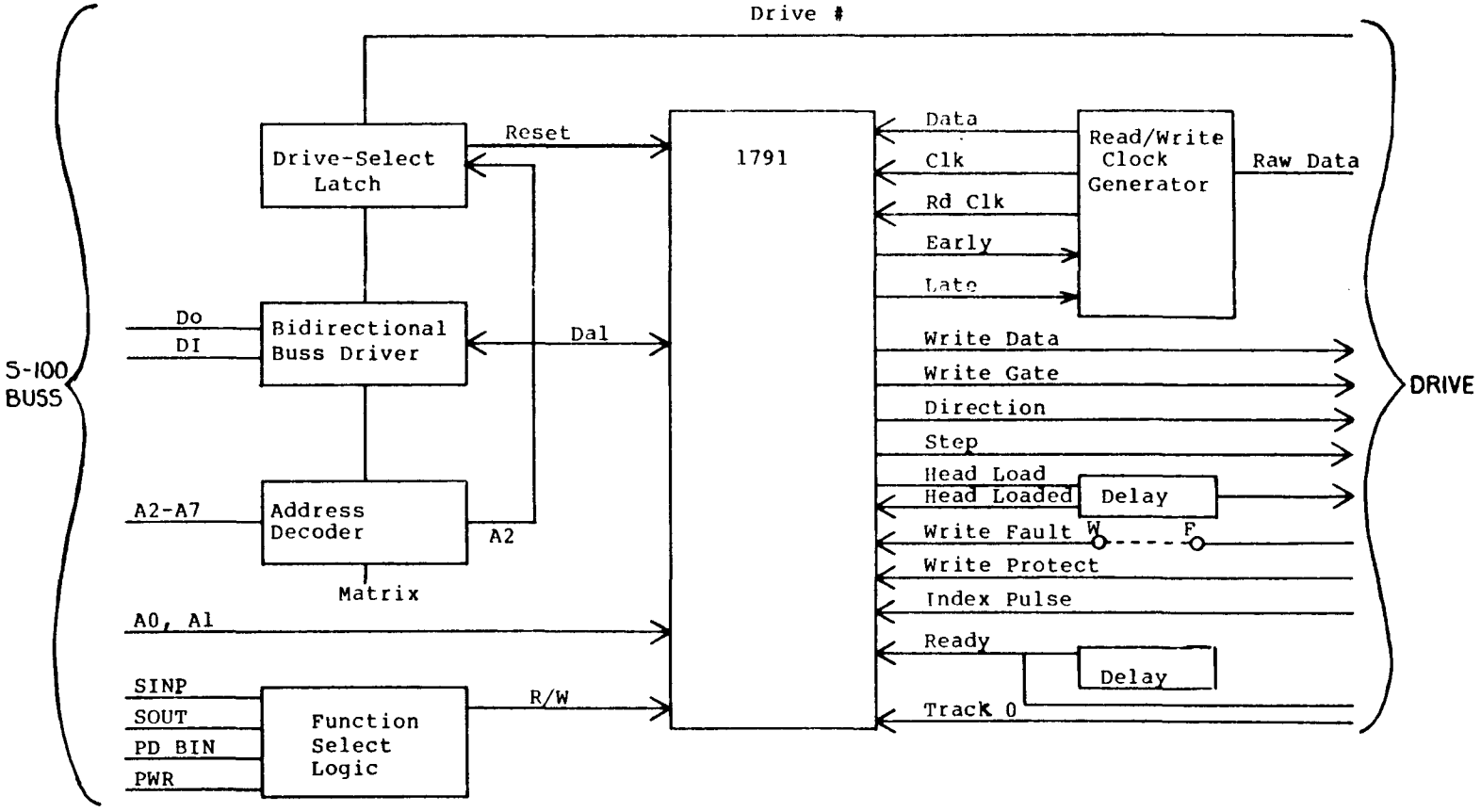


Figure 3-1 FDC-3 Floppy-Disk Controller Card Block Diagram

SECTION III

THEORY OF OPERATION

The TEI, Inc. FDC-3 Floppy-Disk Controller Card (Figure 3-1) contains an Address Decoder, Drive-Select Latch, Function-Select Latch, Bidirectional Bus Buffers, crystal-controlled Read/Write Clock Generator with Digital Phase-Locked loop, type 1791 MOS LSI controller, and miscellaneous logic.

3.1 ADDRESS DECODER

The basic FDC-3 address is XXOY to XXFY (hex) where XX is "don't-care" (high-order address byte not decoded on FDC-3 card), O to F is jumper-selected on the FDC-3 card, and Y is partly jumpered and partly software-controlled to direct the accompanying data byte to the proper card or 1791 device register (Section 3.6).

Comparator Z26 and gates in Z24 and Z25 form the FDC-3 address decoder. The three-row by five-column matrix between Z26 and the card edge enables the jumper selection described above (and in Section 3.8).

When the CPU sends data to the address selected by the jumpers, the Address Decoder enables the card to receive or transmit data.

3.2 DRIVE-SELECT LATCH

Z30 and gates in Z24 and Z25 form an eight-bit latch for the selected drive numbers, type (mini or standard), side number, density, and reset.

Data on the data bus (low order byte with TEI, Inc. CPU-85 card) enters the latch when the operating system executes an OUT instruction to the FDC-3 address, with address bit A2 high. Bits A1 and A0 are ignored.

3.3 FUNCTION-SELECT LOGIC

Gates in Z9, Z24 and Z25 decode CPU commands to the FDC-3 to steer or condition onboard logic to receive or transmit the proper data.

3.4 BIDIRECTIONAL BUS BUFFERS

Z28 and Z29 are four-bit bidirectional bus driver/receivers.

Page 3-2 IS BLANK.

3.5 READ/WRITE CLOCK GENERATION

The Read/Write Clock Generator performs the dual function of (1) Accurately separating incoming data and clocks in either FM mode (single density) or MFM mode (double density); and (2) Supplying write clocks for either recording mode.

This logic consists of a crystal-controlled Oscillator, Dividers, Write-Data Delay Generator, multiplexer-controlled Buffers, and Digital Phase-Locked Loop.

3.5.1 OSCILLATOR

R24, R25, X1, and two sections of Z16 form a 16-MHz oscillator. The oscillator output clocks the Divider logic.

3.5.2 DIVIDERS AND MULTIPLEXED BUFFER

Z12 divides the 16-MHz oscillator signal to generate 2, 4 and 8 MHz. Z14 enables one of the four buffers in Z13, steered by density and drive signals. The selected buffer passes the selected frequency --2, 4, 8, or 16 MHz-- to the Digital Phase-Locked Loop.

3.5.3 WRITE-DATA DELAY GENERATOR AND BUFFER

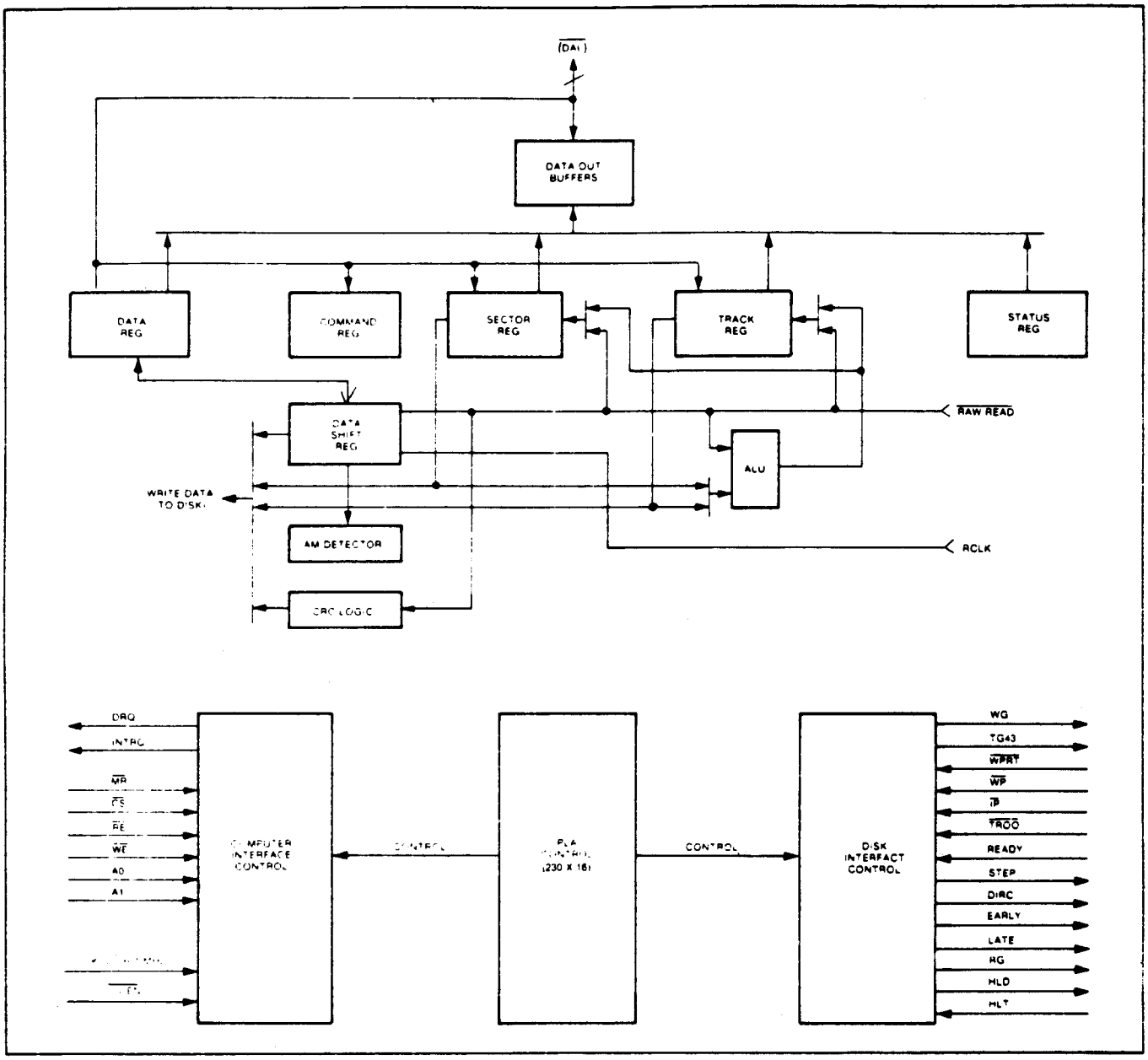
Z5 delays the Write Data signal one, three or five 16-MHz clock times as required for write precompensation. Z14 enables one of the four buffers in Z6, steered by Early and Late outputs from the 1791 device.

3.5.4 DIGITAL PHASE-LOCKED LOOP

Z1, Z2, Z4, Z10, Z11 and Z16 form a Digital Phase-Locked loop. This circuit receives combined data and clock transitions from the drive electronics and accurately separates the clock pulses from the data pulses.

Z1A and Z2A synchronize incoming signal transitions with the FDC-3 clock. Z2B and gates in Z10 output short pulses for each input transition. These pulses clock Z11 and Z4 which output the Read Clock.

Z1B, Z2B, and buffers in Z16 and Z17 select the 1791 device clock.



FD1791 BLOCK DIAGRAM

Figure 3-2 1791 Device Block Diagram

3.6 1791 CONTROLLER

The 1791 Controller is an MOS LSI device that contains logic to select a disk track, then record data on that track or read data already recorded.

The 1791 device (Figure 3-2) consists of a buffered Data Register, Data Shift Register, Sector Register, Command Register, Track-Number Register, Status Register, CRC Logic, Address-Detect Logic Arithmetic/Logic Unit (ALU), Computer-Interface Logic, and Drive-Interface Logic.

3.6.1 DATA REGISTER

This bidirectional register receives data or commands from the CPU and transmits data to the CPU.

3.6.2 DATA SHIFT REGISTER

This register receives eight bits of serial data from the drive, then outputs it as one byte to the Data Register; or receives a byte from the Data Register and transmits it as serial data to the drive.

3.6.3 SECTOR REGISTER

This eight-bit register holds the address of the desired sector.

3.6.4 COMMAND REGISTER

This eight-bit register holds the command currently being executed by the 1791 device. The device has 11 commands of four types (Section IV).

3.6.5 TRACK-NUMBER REGISTER

This eight-bit register holds the number of the track over which the Read/Write head is currently positioned. Step and Direction commands from the Drive-Interface logic increment or decrement the register.

3.6.6 STATUS REGISTER

This eight-bit register holds drive status such as ready, write-protected, etc.; and command-result status. Refer to Appendix A.

3.6.7 CRC LOGIC

This logic generates a unique 16-bit check-word for each data transfer from the CPU, and records that word along with the data. When the data is read out, it again passes through the CRC logic. If the check-word generated during the read operation does not match the recorded check-word, the 1791 device enters a CRC error bit in its Status register and stops the Read operation.

3.6.8 ADDRESS-DETECT LOGIC

This logic detects ID, data, or index marks during operation.

3.6.9 ARITHMETIC/LOGIC UNIT

The ALU increments or decrements registers as required.

3.6.10 COMPUTER-INTERFACE AND DRIVE-INTERFACE LOGIC

The Computer-Interface logic receives all control signals from the CPU and selects register data flow accordingly. The Drive-Interface logic processes status signals from the disk drive and control signals from the Computer-Interface logic to control data transfer to and from the drive.

A Programmed Logic Array (PLA) stores the program that controls both the Computer-Interface and Drive-Interface logic blocks.

3.7 MISCELLANEOUS LOGIC

3.7.1 HEAD-LOAD DELAY

Z21 generates a nominal 40-millisecond delay pulse, timed by C18 and R5, each time the 1791 device generates the Head-Load signal. This pulse applied to the 1791 device's HLT input prevents any transfer until the drive head settles on the diskette surface.

3.7.2 DRIVE-READY LOGIC

3.7.2.1 Miniature Drive

Z20 counts index pulses generated by the drive electronics each time the diskette index-hole passes a sensor in the drive. Upon reaching the desired number (Section 1.6); Z20 outputs a RDY signal for the 1791 device.

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3.7.2.2 Regular Drive

The drive electronics generates RDY/ on interface connector pin 22 upon detection of the second index pulse after drive door closed.

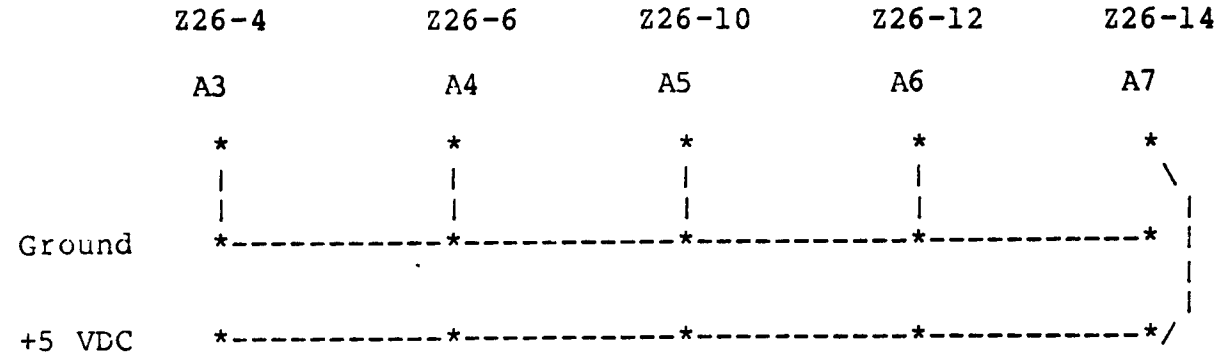


Figure 3-3 FDC-3 Card Address Jumpering, Wiring Side of Card Up

TABLE 3-2
FDC-3 ADDRESS JUMPER SELECTION

	A7	A6	A5	A4
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1
A	1	0	1	0
B	1	0	1	1
C	1	1	0	0
D	1	1	0	1
E	1	1	1	0
F	1	1	1	1

*If A3 strapped high, the low order address byte varies from 8 to F; if low, from 0-7.

3.8 JUMPER SELECTION OF VARIOUS FUNCTIONS

The FDC-3 card has jumper selection for address, interrupts, drive-ready delay, and Write Fault.

The FDC-3 card leaves the factory with etched jumpers selecting these functions for proper operation with the TEI, Inc. Disk Operating System (T/DOS). Changing any of these jumpers may result in improper T/DOS operation.

3.8.1 FDC-3 ADDRESS

Recall from Section 3.1 that the basic FDC-3 address is XXOY to XXFY (hex). Jumpers inserted in the matrix between Z26 and the card edge connector (Figure 3-3) and the System software determine the specific FDC-3 address, 0Y to FY.

The card leaves the factory wtl A7 connected to +5 VDC (logic 1) and A6-A3 connected to ground (logic 0). This forms address 8X, where X consists of A3 at logic 0 and A2 - A0 software-selected from 0-7, which results in a final address of 80 to 87.

To select a different address, refer to Table 3-2, determine the address connection, carefully cut the factory jumpers to Z26 (as required), then solder jumpers from the +5VDC or ground rows to the Z26 inputs.

3.8.2 END-OF-COMMAND INTERRUPT

With the etched jumper just above S-100 bus pin 9 intact, the 1791 device generates a VI5/ interrupt signal at the end of each command.

3.8.3 DATA REQUEST INTERRUPT

With the etched jumper just above pin 10 intact, the 1791 device generates a VI6/ (Data Request) interrupt signal if (1) Data Register full during Read, or (2) Data Register empty during Write.

3.8.4 WRITE FAULT

If the user's drive supplies a Write-Fault signal (WF/), connecting a jumper between points "W" and "F" below the large signal-cable connector causes the 1791 device to stop the Write operation and set the Write-Fault status bit upon detection of the Fault signal.

3.8.5 DRIVE-READY DELAY SELECTION

With the etched jumper (on back side of board) connected to Z20, pin 11 (Figure 3-4), the 1791 device receives a Ready signal after the sixth diskette rotation (sixth index pulse received).

To select the fifth, seventh, or eighth rotation instead, turn the board wiring side up, locate the group of empty holes shown in detail (as asterisks) in Figure 3-4 (approximately 3" (7.5 cm) straight down from left edge of large signal connector), cut the etched jumper, then solder a jumper from the single hole to the hole above pin 10 for selection of the fifth rotation, to the hole above pin 12 for selection of the seventh rotation, or to the hole above pin 13 for selection of the eighth rotation.

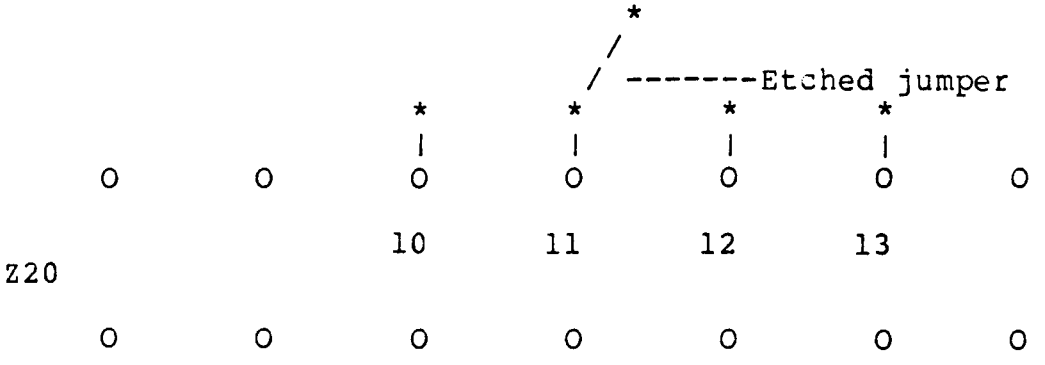


Figure 3-4 Drive-Ready Delay Jumper Selection, Wiring Side

SECTION IV

SOFTWARE CONSIDERATIONS

4.1 FDC-3 CARD

The FDC-3 card requires three programming steps: Drive Selection, Drive Initialization, and Data Transfer. The TEI, Inc. Operating System, T/DOS Version 2.0 (or higher), performs these functions as required for program operation. Note that T/DOS Versions 2.0 - 2.XX support a maximum of four diskette drives.

4.2 1791 DEVICE

The 1791 LSI device responds to 11 commands of four types. Type I commands cause head and/or stepper motor action. Type II commands read or write data from/to a selected sector. Type III commands read an address or data from a track or write data onto a track. The single Type IV command controls the device's interrupt capabilities.

As stated for the FDC-3 card, T/DOS supplies these commands as needed for program operation.

Refer to Appendix A for a discussion of 1791 device commands and status codes.

SECTION V

HARDWARE CONSIDERATIONS

5.1 DRIVE CONFIGURATION

Each drive in a TEI, Inc. Computer System must be physically configured according to its System designation. Configuration occurs during System checkout.

Drive selection during program operation is software-controlled.

5.2 SIGNAL-CABLE CONNECTIONS

5.2.1 REGULAR DRIVES

Table 5-1 shows signal connections for regular drives (large connector).

5.2.2 MINIATURE DRIVES

Table 5-2 shows signal connections for miniature drives (small connector).

TABLE 5-1
REGULAR DRIVE SIGNAL CONNECTIONS

Pin	FUNCTION	Pin	FUNCTION
1	Ground	26	Enable Drive Select 1
2	Spare	27	Ground
3	Ground	28	Drive Select 2
4	Write Fault	29	Ground
5	Ground	30	Drive Select 3
6	Track 44-76	31	Ground
7	Ground	32	Drive Select 4
8	Spare	33	Ground
9	Ground	34	Direction
10	Spare	35	Ground
11	Ground	36	Step
12	Not Used	37	Ground
13	Ground	38	Write Data
14	Side Select	39	Ground
15	Ground	40	Write Gate
16	In Use*	41	Ground
17	Ground	42	Spare
18	Head Load	43	Ground
19	Ground	44	Write Protect
20	Index	45	Ground
21	Ground	46	Raw Data
22	Ready	47	Ground
23	Ground	48	Separated Data
24	Spare	49	Ground
25	Ground	50	Separated Clock

* Door Light

TABLE 5-2
MINIATURE DRIVE SIGNAL CONNECTION

Pin	FUNCTION	Pin	FUNCTION
1	Ground	18	Direction
2	Spare	19	Ground
3	Ground	20	Step
4	Spare	21	Ground
5	Ground	22	Write Data
6	Spare	23	Ground
7	Ground	24	Write Gate
8	Index	25	Ground
9	Ground	26	Track 0
10	Drive 1 Select	27	Ground
11	Ground	28	Write Protect
12	Drive 2 Select	29	Ground
13	Ground	30	Raw Data
14	Drive 3 Select	31	Ground
15	Ground	32	Side Select
16	Motor On	33	Ground
17	Ground	34	

SECTION VI

USER REPAIR GUIDE

TEI, Inc. designed and built your FDC-3 Floppy-Disk Controller Card for extreme reliability. Before returning the card for repair, please check the following items:

1) Does power-supply fan run and memory-size prompt appear on screen when System turned on and Operating System diskette loaded into drive? If not, check computer AC connection and fuse. **TURN POWER OFF AND UNPLUG LINE CORD FIRST.**

2) Is card seated properly? Turn power off, pull up on inside edge of both card ejectors (Figure 6-1) simultaneously to unseat card, then press firmly back into socket.

   If card still does not function properly, unplug signal cable(s), unseat card as described above, remove unseated card carefully from Computer, then place card on a clean, firm surface and GENTLY burnish each contact on both sides of the S-100 bus edge connector with a pencil eraser. Do not use a power eraser or an art gum eraser. Replace card in Computer, then reconnect signal cable(s). Be sure to seat both card and connector(s) firmly.

3) Is each diskette-drive signal cable seated properly? Turn power off, press firmly in on cable connector.

4) Does problem exist for one diskette only? If so, copy as much material as possible from defective diskette to good diskette and discard bad diskette.

5) In multidrive Systems, does problem exist for one drive only? Check that motor in problem drive turns by looking into drive with door open.

If all above items check and FDC-3 card still does not function correctly, please contact:

Customer Support Coordinator
TEI, Inc.
5075 South Loop East
Houston, TX 77033 USA
(713) 738-2300
TWX: 910-881-3639

APPENDIX A

TEI, INC. T/DOS DISKETTE READ/WRITE ERROR INDICATIONS

A.1 GENERAL

For each diskette-drive action required by T/DOS, the 1791 device receives an eight-bit command code. After each action, the 1791 device returns an eight-bit Status code. The Status-code meaning depends on the command. In case of an error, T/DOS displays both codes, plus numbers of track and sector where error occurred, as follows:

READ/WRITE ERROR:
STATUS = X1X2, TRACK = X1X2, SECTOR = X1X2, COMMAND = X1X2

where "X1X2" is two hexadecimal (base 16) digits.

T/DOS forms hexadecimal digits from the Status or Command codes as follows:

High-Order Digit				Low-Order Digit			
C7	C6	C5	C4	C3	C2	C1	C0
S7	S6	S5	S4	S3	S2	S1	S0

A.2 COMMANDS

The 1791 device responds to 11 commands of four types.

A.2.1 TYPE I COMMANDS

Type I commands cause diskette read/write head motion. Table A-1 shows the Type I commands and associated codes.

TABLE A-1
TYPE I COMMAND CODES

COMMAND	CODE (HEX)
Restore	00-0F
Seek	10-1F
Step-In	40-4F; 50-5F
Step-Out	60-6F; 70-7F
Step	20-2F; 30-3F

Status codes are as follows:

S7 1 = Drive Ready; 0 = Drive not ready
S6 1 = Drive Write-Protected; 0 = Drive not Write-Protected
S5 1 = Head Loaded; 0 = Head unloaded
S4 1 = Track Number not Verified; 0 = Track Number Verified
S3 1 = CRC Error; 0 = No CRC Error
S2 1 = Head over Track 0; 0 = Head not over Track 0
S1 1 = Index pulse detected; 0 = No index pulse detected
S0 1 = Command in progress, device Busy; 0 = no command in progress, device idle

If S7 set, T/DOS writes DRIVE NOT READY on the screen. If S6 set, T/DOS writes WRITE PROTECTED on the console screen. S4 is not checked. If S3 set, T/DOS generates an error message with status 08. S2 - S0 set are not errors.

A.2.2 TYPE II AND TYPE III COMMANDS

Type II commands cause reading or writing data from/to the sector selected by a preceding Type I command. Table A-2 shows the Type II command codes.

Type III commands read or write data from a selected track. The Read Address command reads the first ID field from a selected track, then loads the track address into the 1791 Sector Register. The Read Track command reads every data byte, including address marks, gap marks, etc., from the selected track. The Write Track command writes data bytes on the selected track.

Table A-3 shows command codes.

TABLE A-2
TYPE II COMMAND CODES

COMMAND	CODE (HEX)
Read	80-8C; 90-9C
Write	A0-AF; B0-BF

TABLE A-3
TYPE III COMMAND CODES

COMMAND	CODE (HEX)
Read Address	C4
Read Track	E4
Write Track	F4

Both command types have status codes as follows:

S7 1 = Drive Ready
S6 1 = Drive Write-Protected
S5 1 = Record Data Mark deleted, Read Sector command; Write Fault, Write Command.
S4 1 = Record not found.
S3 1 = CRC Error
S2 1 = Lost data. Computer did not respond in time.
S1 1 = Read Command: Data register full; Write Command: Data Register empty
S0 1 = Command in progress, device Busy

Unless the drive becomes not-ready after track selection, status bit 7 should always be logic 1. Similarly, status bit 6 should always be logic 0, unless diskette becomes write-protected after track selection.

S5 at logic 1 is not an error for a Read operation. For a Write operation, it causes T/DOS to give an error message with status code equal to one of 40 - 4F. S4 at logic 1 causes T/DOS to write SEEK ERROR on the console screen. S3 at logic 1 causes T/DOS to give an error message with status 08. S2 at logic 1 causes T/DOS to give an error message with status 04. S1 and S0 are not considered errors.

A.2.4 TYPE IV COMMAND

The single Type IV command, Force Interrupt, causes the 1791 device to generate an interrupt to the host CPU immediately, or upon completion of certain specified conditions. If received while any Type I, II, or III command executing, the Type IV command resets the S0 status bit, but leaves S1 - S7 unchanged. If received at any other time, the Type IV command resets S0 and updates or resets S1 - S7.

The Type IV command generates no error messages.

A.3 ERROR RECOVERY PROCEDURES

A.3.1 ENGLISH-LANGUAGE ERROR MESSAGES

These messages and associated recovery procedures are discussed in detail in the T/DOS (TEI, Inc. Disk Operating System) Systems Reference Manual, TEI, Inc. part number 15092.

A.3.2 CODED ERROR MESSAGES

The following is list of possible coded error messages. A detailed explanation of each concludes this Section.

80 = Drive not ready
40 = Write Protected
20 = Write Fault
10 = Seek Error, or Not Found
08 = CRC Error
04 = Lost Data

A.3.2.1 Status = 80

The "80" error occurs if a drive becomes not-ready at some time other than before track selection. Not-ready at selection time should have caused DRIVE NOT READY message to appear. Status 80 might occur if drive worn, if diskette accidentally removed while System operating, or if drive electronics fail.

To recover, if diskette accidentally removed, replace it, then reboot System; otherwise, just open and close diskette drive door. If problem remains, refer to Section VI.

A.3.2.2 Status = 40

The "40" error occurs if a drive becomes write-protected during operation. This could occur if an 8" diskette write-protect tab fell off due to poor adhesive quality, or if drive electronics failure occurs.

To recover, check the diskette tab (8" diskette only). If problem remains, refer to Section VI.

A.3.2.3 Status = 20

The "20" error occurs if a Write error occurs and the "W" and "F" points are connected together on the FDC-3 card.

Typing "R" causes T/DOS to Retry the operation four times. If the error recurs, try pressing R again. If the error does not go away after several retries, refer to Section VI.

A.3.2.4 Status = 10

The "10" error occurs if the drive or controller cannot find the program-selected track/sector combination.

Typing "R" causes T/DOS to Retry the operation four times. If the error recurs, try pressing R again. If the error does not go away after several retries, refer to Section VI.

A.3.2.5 Status = 08

The "08" error occurs if CRC (Section 3.6.7) does not check on a data field.

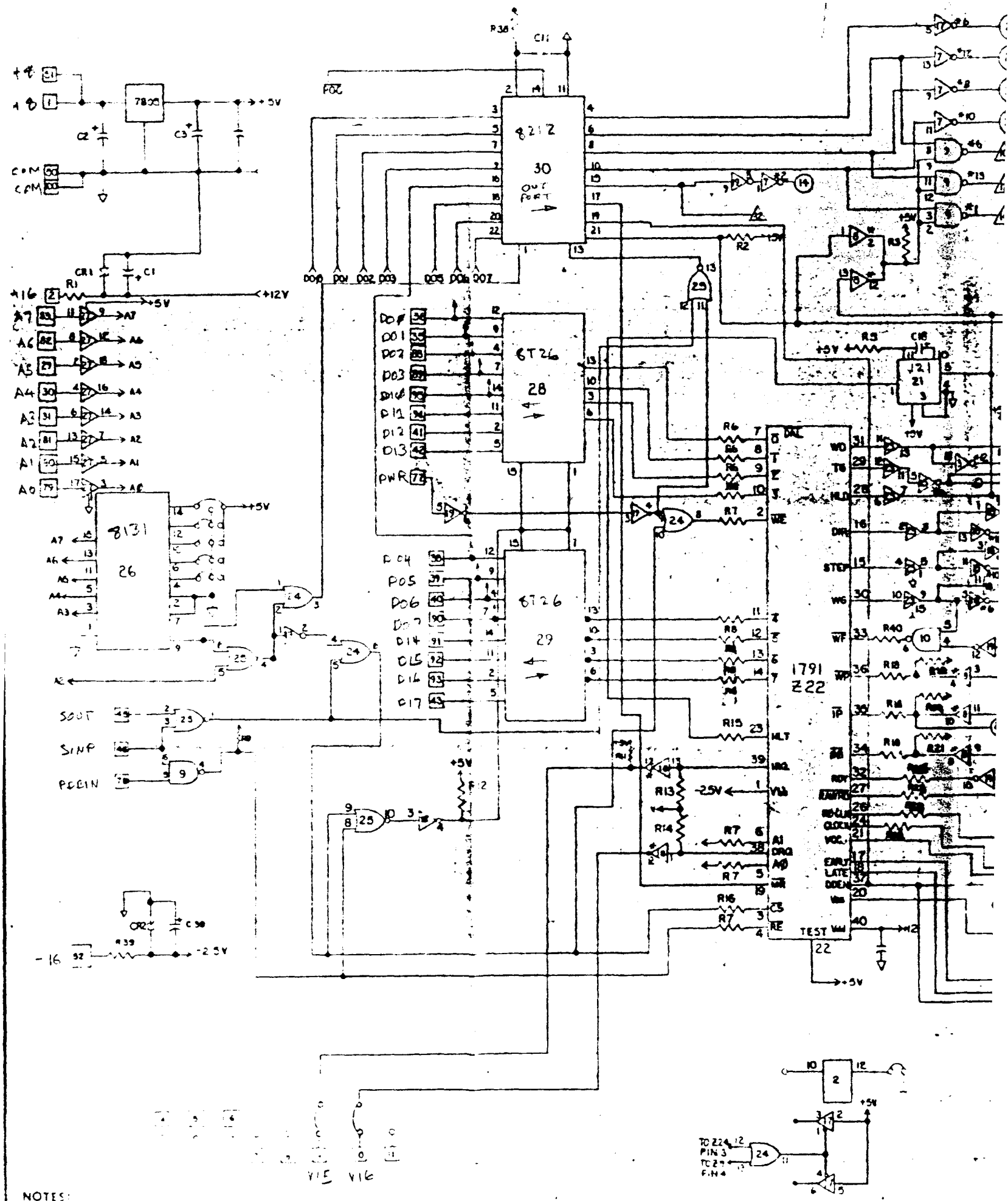
Recovery from status 08 messages may or may not be possible. With an Word Processing Program in operation, try the Save procedure, then retry the file. If the error recurs, go to the backup file.

If a backup file is not available, typing "R" causes T/DOS to Retry the operation four times. If the error recurs, try pressing R again. If the error does not go away after several retries, press RETURN. T/DOS now ignores the error; however several errors in the same sector may cause the BDOS ERROR ON BAD SECTOR message to appear.

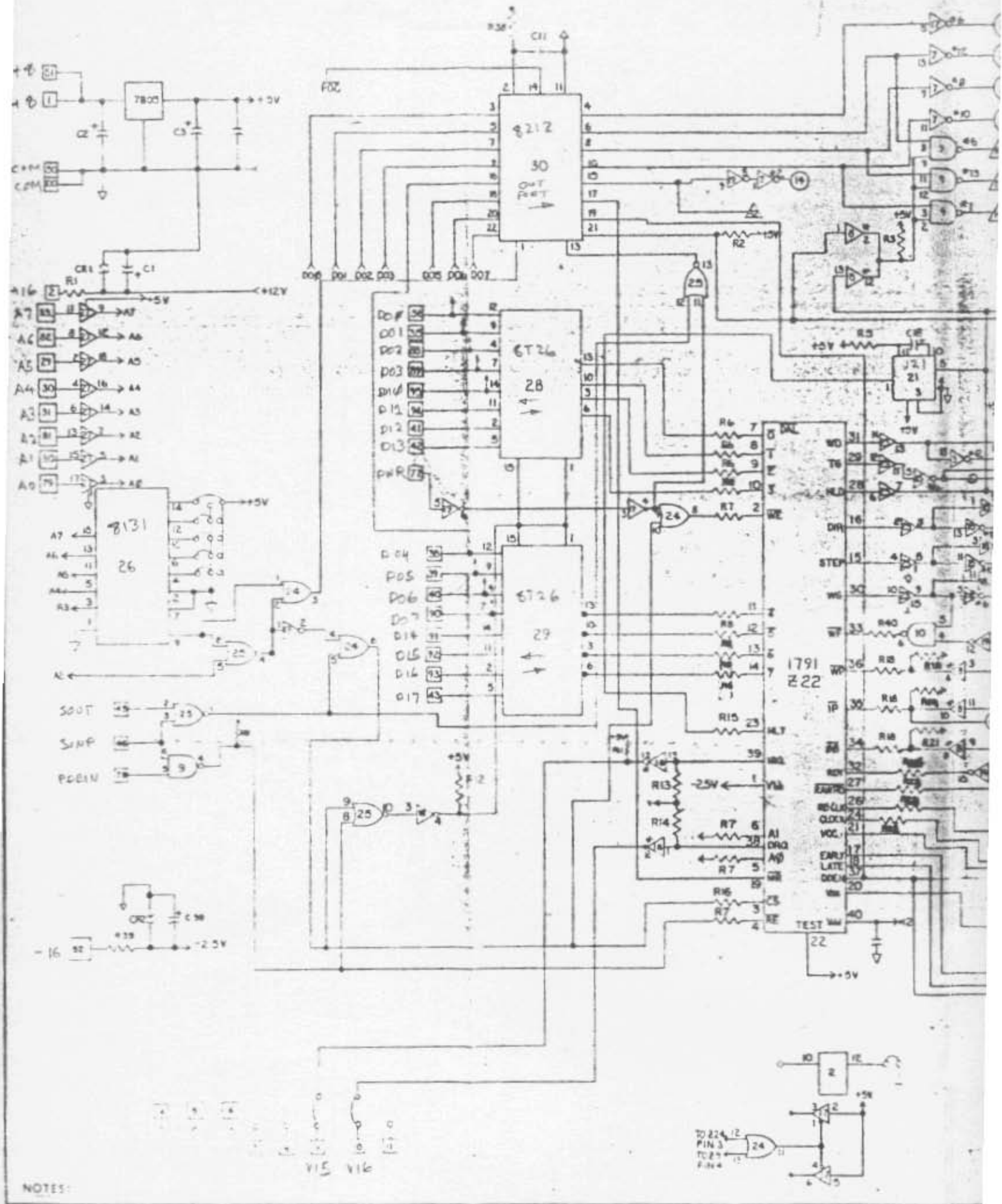
If the error is a data error, some or all the nearby text/data may be lost. Transfer as much data as possible to another diskette, and discard the original diskette. If the error is a disk-formatting error, data may be intact. Transfer as much as possible to another diskette, reformat the original diskette, and try using it again.

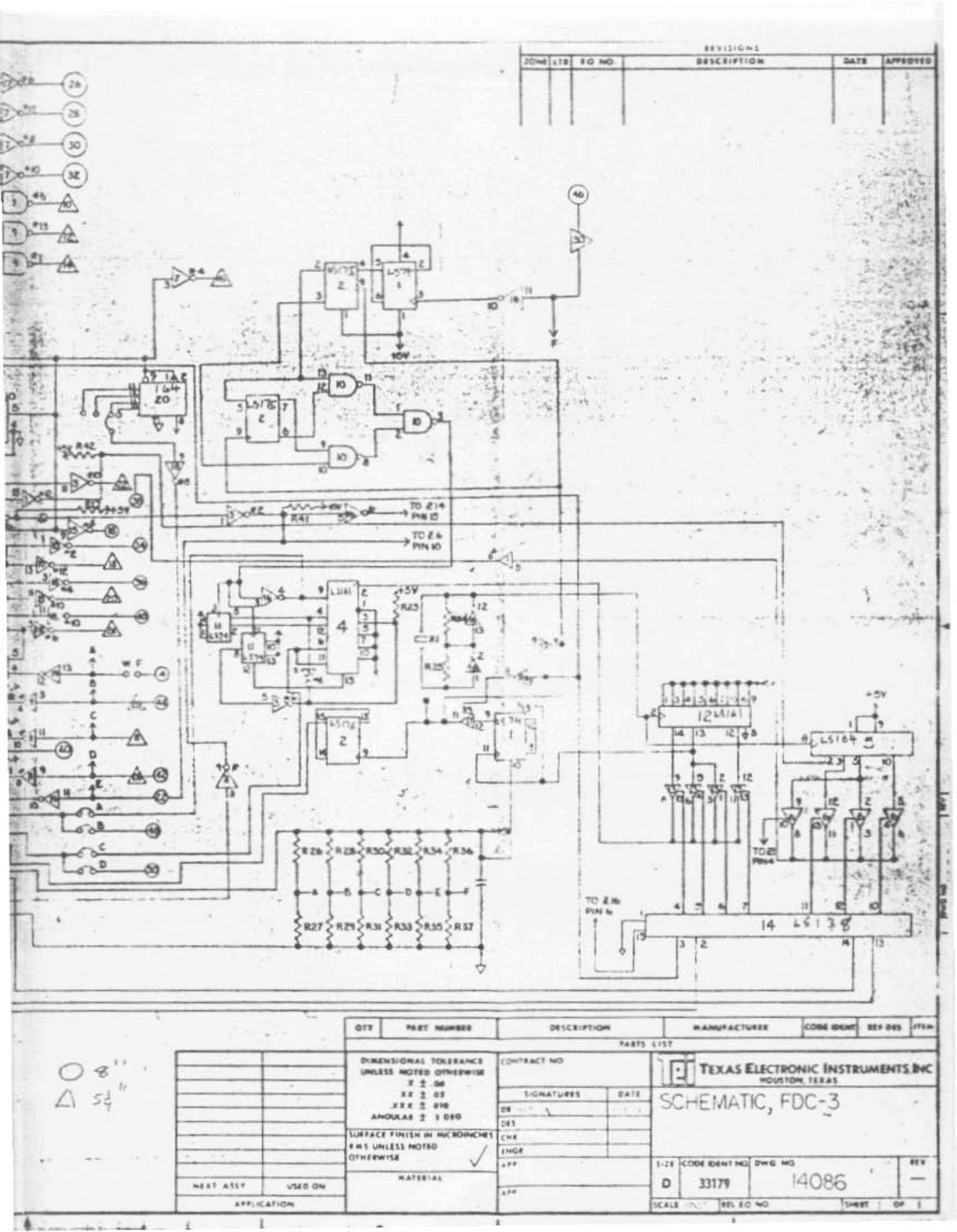
A.3.2.6 Status = 04

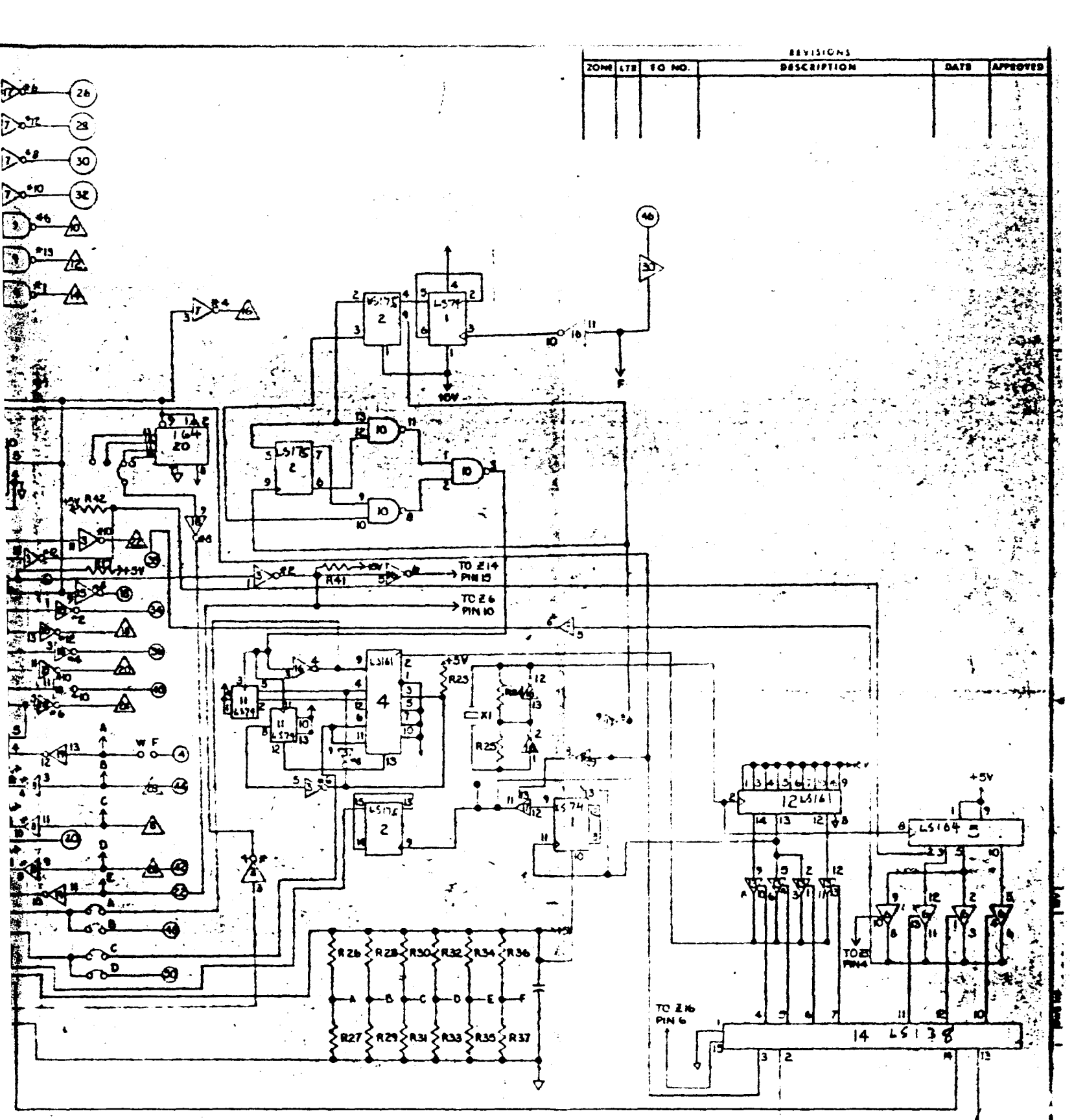
The "04" message occurs if data lost because the CPU did not transfer it in time. Refer to Section VI.


7805
+5V
COM
8212
30
OUT PORT
8T26
28
8T26
29
8131
26
1791
Z22
+12V
-5V
-2.5V
SOUT
SINP
PCBIN
TEST
TO Z24 PIN 3
TO Z9 PIN 4

NOTES:


7805
+5V
+12V
-2.5V
8212
30
8T26
28
8T26
27
8131
26
1791
Z22
TEST
22
NOTES:


REVISIONS
ZONE | LTR | E.O. NO. | DESCRIPTION | DATE | APPROVED
TO Z14 PIN 10
TO Z6 PIN 10
TO Z6 PIN 4
TO Z14 PIN 4
R41
R42
R23
R25
R26
R28
R30
R32
R34
R36
R27
R29
R31
R33
R35
R37
+5V
10V
PARTS LIST
QTY | PART NUMBER | DESCRIPTION | MANUFACTURER | CODE IDENT | REV DES | ITEM
DIMENSIONAL TOLERANCE UNLESS NOTED OTHERWISE
X ± .06
XX ± .03
.XXX ± .010
ANGULAR ± 3 DEG
SURFACE FINISH IN MICROINCHES RMS UNLESS NOTED OTHERWISE
MATERIAL
CONTRACT NO
SIGNATURES | DATE
DR
DES
CHK
ENGR
APP
APP
NEXT ASSY | USED ON
APPLICATION
TEXAS ELECTRONIC INSTRUMENTS INC
HOUSTON, TEXAS
SCHEMATIC, FDC-3
SIZE D | CODE IDENT NO. 33179 | DWG NO. 14086 | REV —
SCALE NONE | REL E.O. NO. | SHEET 1 OF 1



QTY	PART NUMBER	DESCRIPTION	MANUFACTURER	CODE IDENT	REF DES	ITEM

PARTS LIST

NEXT ASSY	USED ON
APPLICATION	

DIMENSIONAL TOLERANCE UNLESS NOTED OTHERWISE
X ± .06
XX ± .02
.XXX ± .010
ANGULAR ± 5 DEG

SURFACE FINISH IN MICROINCHES RMS UNLESS NOTED OTHERWISE ✓

MATERIAL

CONTRACT NO

SIGNATURES	DATE
DR	
DES	
CHK	
ENGR	
APP	
APP	

TEXAS ELECTRONIC INSTRUMENTS, INC
HOUSTON, TEXAS

SCHEMATIC, FDC-3

SIZE	CODE IDENT NO.	DWG NO.	REV
D	33179	14086	—

SCALE | REL EO NO | SHEET 1 OF 1

○ 8"
△ 5¼"